IN THE SPECIFICATION

[0053] Like transistors 110 and ~~130~~ 120, programming transistor 130 includes a source 128, a drain 129, a channel region 127 between source 128 and drain 129, a floating gate 121 above channel region 127 (and electrically connected to floating gate 111 of storage transistor 110), a control gate 122 above floating gate 121, and oxide layers 123 and 124 between channel region 127 and floating gate 121, and between floating gate 121 and control gate 122, respectively.

[0060] For example, programming circuit 170 shown in Fig. 3 includes programming logic 171, an AND gate 172, and erase logic 173. AND gate 172 is coupled to receive programming signal SET and control signal CTRL, and programming logic ~~172~~ 171 is coupled to receive the output of AND gate ~~171~~ 172 and a high voltage V_HI and provide programming voltage V_PRG, while erase logic 173 is coupled to receive erase signal RETUNE and high voltage V_HI and provide erase voltage V_ERS.

[0062] Output control circuit 190 includes an inverter 191 coupled to receive comparator output signal CMP and provide control signal CTRL as an output, a NAND gate 192 coupled to receive as inputs signals /SET and /RETUNE (i.e., the complements of programming signal SET and erase signal RETUNE, respectively), and a NOR gate 193 coupled to receive as inputs the output of inverter 191 and ~~control signal CTRL~~ the output of NAND gate 192, and provide output signal V_OUT as an output. Finally, comparator 180 includes a differential comparator 180A, which is described in greater detail below.